CS33

NEW SCHEME

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Third Semester B.E. Degree Examination, January/February 2004

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *1.Answer any FIVE full questions.*
2.All questions carry EQUAL marks.

1. (a) Explain the principle of duality. (4 Marks)

   (b) Mention two categories of Boolean expressions based on their structure. Write these forms for any give three - variable function $T(x, y, z)$. (8 Marks)

   (c) Give the Shanon's expansion theorem. (4 Marks)

   (d) Explain the exclusive-or-function. (4 Marks)

2. (a) Design an odd parity bit generator using gates for the decimal digits 0 to 9 represented in 84.21 BCD. Give the necessary truth table and draw the logic diagram. Explain. (8 Marks)

   (b) What code is used to label the row headings and column headings of a Karnaugh map and why? (4 Marks)

   (c) Using K-map obtain the minimal sum of products and the minimal product of sums form of the funciton $f(a, b, c, d) = \Sigma m(1, 2, 3, 5, 6, 7, 8, 13)$ (8 Marks)

3. (a) Mention one advantage and one disadvantage of the Quine-McCluskey method for obtaining the prime implicants of a given Boolean function. Obtain all the prime implicants of the function.

   $$f(v, w, x, y, z) = \Sigma m(4, 5, 9, 11, 12, 14, 15, 27, 30) + dc(1, 17, 25, 26, 31)$$

   Use Quinne-McCluskey method. Do you have any essential prime implicants. (12 Marks)

   (b) In what way MEV-K-map differs from the conventional K-maps? Simplify the function

   $$f(a, b, c, d) = \Sigma_m(2, 3, 4, 5, 13, 15) + dc(8, 9, 10, 11)$$

   using a two variable MEV-K-map. (8 Marks)

4. (a) With the aid of a neat circuit diagram explain the operation of a 2-input TTL nand gate with totem output. (8 Marks)

   (b) Discuss how a resistor could be constructed using MOSFET. Give the resistor characteristics. (6 Marks)

   (c) Draw the NMOS as well as PMOS circuit diagrams to realise a NAND gate. Give the relevant truth tables. (6 Marks)

5. (a) Explain a 4 bit parallel adder with the carry look ahead scheme. Clearly indicate how this scheme improves the performance of the operation. (10 Marks)

   (b) With the aid of block diagrams clearly distinguish between a decoder and encoder. (4 Marks)

   (c) Give a 4-to-1 MUX implementation of the three variable function

   $$f = \Sigma m(1, 4, 5, 7)$$ (6 Marks)

6. (a) Illustrate how a PLA can be used for combinational logic design with reference to the functions.

$f_1(a,b,c) = \Sigma m(0,1,3,4)$

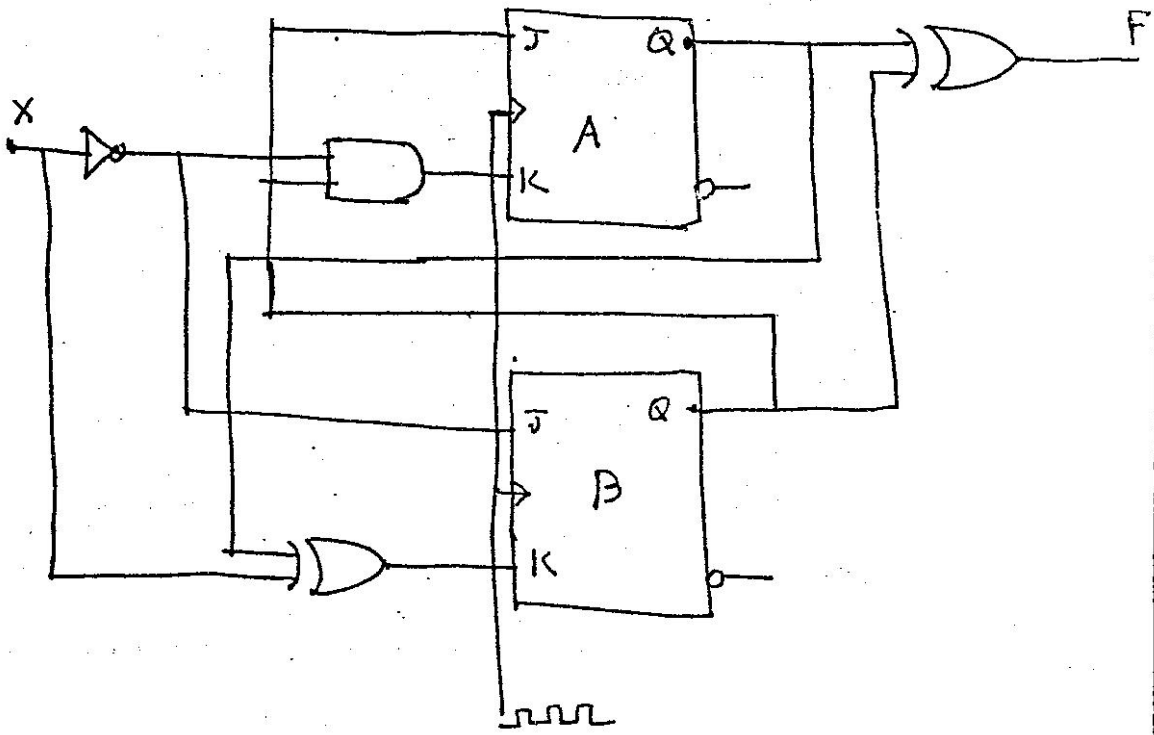
$f_2(a,b,c) = \Sigma m(1,2,3,4,5)$

Realize the same assuming, that a 3 x 4 x 2 PLA is available. (10 Marks)

(b) Give the details of a master slave S-R flip flop. Draw the logic diagram. Explain the flip flop action during the control signal. Also give the function table. (10 Marks)

7. (a) Draw the block diagram of a mod-7 twisted ring counter and explain its operation. Give the count sequence table and the decoding logic used to identify the various states. (10 Marks)

(b) Construct the excitation table, transition table and state diagram for the Moore sequential circuit given below: (10 Marks)



8. Write notes on:
   (a) 1 - bit comparator
   (b) Fan - in and Fan out
   (c) Integration levels of IC's
   (d) Binary full subtractor. (4×5=20 Marks)

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